Viterbi Decoder Vhdl Code

The Asia and South Pacific conference on design automation is the second in a series of biennial international conferences. It aims to provide the CAD/DA community with the opportunity to present ideas and concepts on upperstream design as well as methodologies of downstream design.

Since the invention of wireless telegraphy by Marconi in 1897, wireless technology has not only been enhanced, but also has become an integral part of our everyday lives. The first wireless mobile phone appeared around 1980. It was based on first generation analog technology that involved the use of Frequency Division Multiple Access (FDMA) techniques. Ten years later, second generation (2G) mobiles were dependent on Time Division Multiple Access (TDMA) techniques and Code Division Multiple Access (CDMA) techniques. Nowadays, third generation (3G) mobile systems depend on CDMA techniques to satisfy the need for faster, and more capacious data transmission in mobile wireless networks. Wideband CDMA (WCDMA) has become the major 3G air interface in the world. WCDMA employs convolutional encoding to encode voice and MPEG4 applications in the baseband transmitter at a maximum frequency of 2Mbps. To decode convolutional codes, Andrew Viterbi invented the Viterbi Decoder (VD) in 1967. In 2G mobile terminals, the VD consumes approximately one third of the power consumption of a baseband mobile transceiver. Thus, in 3G mobile systems, it is essential to reduce the power consumption of the VD. Conceptually, the Register Exchange (RE) method is simpler and faster than the Trace Back (TB) method for implementing the VD. However, in the RE method, each bit in the memory must be read and rewritten for each bit of information that is decoded. Therefore, the RE method is not appropriate for decoders with long constraint lengths. Although researchers have focused on implementing and optimizing the TB method, the RE method is focused on and modified in this thesis to reduce the RE method's power consumption. This thesis proposes a novel modified RE method by adopting a pointer concept for implementing the survivor memory unit (SMU) of the VD. A pointer is assigned to each register or memory location. The contents of thepointer which points to one register is altered to point to a second register, instead of copying the contents of the first register to the second. When the pointer concept is applied to the RE's SMU implementation (modified RE), there is no need to copy the contents of the SMU and rewrite them, but one row of memory is still needed for each state of the VD. Thus, the VDs in CDMA systems require 256 rows of memory. Applying the pointer concept reduces the VD's power consumption by 20 percent as estimated by the VHDL synthesis tool and by the new power reduction estimation that is introduced in this work. The coding gain for the modified RE method is 2.6dB at an SNR of approximately 10-3. Furthermore, a novel zero-memory implementation for the modified RE method is proposed. If the initial state of the convolutional encoder is known, the entire SMU of the modified RE VD is reduced to only one row. Because the decoded data is generated in the required order, even this row of memory is dispensable. The zero-memory architecture is called the MemoryLess Viterbi Decoder (MLVD), and reduces the power consumption by approximately 50 percent. A prototype of the MLVD with a one third convolutional code rate and a constraint length of nine is mapped into a Xilinx 2V6000 chip, operating at 25 MHz with a decoding throughput of more than 3Mbps and a latency of two data bits. The other problem of the VD which is addressed in this thesis is the Add Compare Select Unit (ACSU) which is composed of 128 butterfly ACS modules. The ACSU's high parallelism has been previously solved by using a bit serial implementation. The 8-bit First Input First Output (FIFO) register, needed for the storage of each path metric (PM), is at the heart of the single bit serial ACS butterfly module. A new, simply controlled shift register is designed at the circuit level and integrated into the ACS module. A chip for the new module is also fabricated.

Quick-Turnaround ASIC Design in VHDL

VHDL User's Forum in Europe

Science Abstracts

Proceedings

Electrical & electronics abstracts. Series B

Proceedings of IEEE Region 10 International Conference on Electrical and Electronic Technology

Details a real-world product that applies a cutting-edge multi-core architecture Increasingly demanding modern applications—such as those used in telecommunications networking and real-time processing of audio, video, and multimedia streams—require multiple processors to achieve computational performance at the rate of a few giga-operations per second. This necessity for speed and manageable power consumption makes it likely that the next generation of embedded processing systems will include hundreds of cores, while being increasingly programmable, blending processors and configurable hardware in a power-efficient manner. Multi-Core Embedded Systems presents a variety of perspectives that elucidate the technical challenges associated with such increased integration of homogeneous (processors) and heterogeneous multiple cores. It offers an analysis that industry engineers and professionals will need to understand the physical details of both software and hardware in embedded architectures, as well as their limitations and potential for future growth. Discusses the available programming models spread across different abstraction levels The book begins with an overview of the evolution of multiprocessor architectures for embedded applications and discusses techniques for autonomous power management of system-level parameters. It addresses the use of existing open-source (and free) tools originating from several application domains—such as traffic modeling, graph theory, parallel computing and network simulation. In addition, the authors cover other important topics associated with multi-core embedded systems, such as: Architectures and interconnects Embedded design methodologies Mapping of applications

Compendio de los trabajos presentados en Toledo durante el VHDL user's forum in Europe.

Proceedings, Seventh IEEE International Workshop on Rapid System Prototyping

A Hierarchical, Automated Design Flow for Low-power, High-throughput Digital Signal Processing IC's

VLSI: Integrated Systems on Silicon

ICECS

Advances in Computer Science, Environment, Ecoinformatics, and Education, Part III

Low Power Techniques for Implementing a Viterbi Decoder

From the Foreword..... Modern digital signal processing applications provide a large challenge to the system designer. Algorithms are becoming increasingly

complex, and yet they must be realized with tight performance constraints. Nevertheless, these DSP algorithms are often built from many constituent canonical subtasks (e.g., IIR and FIR filters, FFTs) that can be reused in other subtasks. Design is then a problem of composing these core entities into a cohesive whole to provide both the intended functionality and the required performance. In order to organize the design process, there have been two major approaches. The top-down approach starts with an abstract, concise, functional description which can be quickly generated. On the other hand, the bottom-up approach starts from a detailed low-level design where performance can be directly assessed, but where the requisite design and interface detail take a long time to generate. In this book, the authors show a way to effectively resolve this tension by retaining the high-level conciseness of VHDL while parameterizing it to get good fit to specific applications through reuse of core library components. Since they build on a pre-designed set of core elements, accurate area, speed and power estimates can be percolated to high- level design routines which explore the design space. Results are impressive, and the cost model provided will prove to be very useful. Overall, the authors have provided an up-to-date approach, doing a good job at getting performance out of high-level design. The methodology provided makes good use of extant design tools, and is realistic in terms of the industrial design process. The approach is interesting in its own right, but is also of direct utility, and it will give the existing DSP CAD tools a highly competitive alternative. The techniques described have been developed within ARPAs RASSP (Rapid Prototyping of Application Specific Signal Processors) project, and should be of great interest there, as well as to many industrial designers. Professor Jonathan Allen, Massachusetts Institute of Technology

This book contains the papers that have been presented at the ninth Very Large Scale Integrated Systems conference VLSI'97 that is organized biannually by IFIP Working Group 10.5. It took place at Hotel Serra Azul, in Gramado Brazil from 26-30 August 1997. Previous conferences have taken place in Edinburgh, Trondheim, Vancouver, Munich, Grenoble and Tokyo. The papers in this book report on all aspects of importance to the design of the current and future integrated systems. The current trend towards the realization of versatile Systems-on-a-Chip require attention of embedded hardware/software systems, dedicated ASIC hardware, sensors and actuators, mixed analog/digital design, video and image processing, low power battery operation and wireless communication. The papers as presented in Jhis book have been organized in two tracks, where one is dealing with VLSI System Design and Applications and the other presents VLSI Design Methods and CAD. The following topics are addressed: VLSI System Design and Applications Track • VLSI for Video and Image Processing. • Microsystem and Mixed-mode design. • Communication And Memory System Design • Cow-voltage & Low-power Analog Circuits. • High Speed Circuit Techniques • Application Specific DSP Architectures. VLSI Design Methods and CAD Track • Specification and Simulation at System Level. • Synthesis and Technology Mapping. • CAD Techniques for Low-Power Design. • Physical Design Issues in Sub-micron Technologies. • Architectural Design and Synthesis. • Testing in Complex Mixed Analog and Digital Systems.

International Conference on VLSI and CAD.

Application Specific Integrated Circuits

IEEE International Conference on Personal Wireless Communications

Digital Signal Processors

Proceedings of the ASP-DAC '97, Asia and South Pacific Design Automation Conference 1997, January 28-31, 1997, Makuhari Messe, Nippon Convention Center, Chiba, Japan

A Proceedings Volume from the 5th IFAC Workshop, Gliwice, Poland, 22-23 November 2001

This 5-volume set (CCIS 214-CCIS 218) constitutes the refereed proceedings of the International Conference on Computer Science, Environment, Ecoinformatics, and Education, CSEE 2011, held in Wuhan, China, in July 2011. The 525 revised full papers presented in the five volumes were carefully reviewed and selected from numerous submissions. The papers are organized in topical sections on information security, intelligent information, neural networks, digital library, algorithms, automation, artificial intelligence, bioinformatics, computer networks, computational system, computer vision, computer modelling and simulation, control, databases, data mining, e-learning, e-commerce, e-business, image processing, information systems, knowledge management and knowledge discovering, mulitimedia and its apllication, management and information system, moblie computing, natural computing and computational intelligence, open and innovative education, pattern recognition, parallel and computing, robotics, wireless network, web application, other topics connecting with computer, environment and ecoinformatics, modeling and simulation, environment restoration, environment and energy, information and its influence on environment, computer and ecoinformatics, biotechnology and biofuel, as well as biosensors and bioreactor.

These volumes contain the conference proceedings from the IEEE Region 10 International Conference on Electrical and Electronic Technology.

Field-Programmable Logic and Applications: Reconfigurable Computing Is Going Mainstream

Town and Country Hotel, May 16-19, 1999, San Diego, California

Proceedings of the IEEE 1999 Custom Integrated Circuits Conference

CISIS'09, 2nd International Workshop Burgos, Spain, September 2009 Proceedings

BMAS ...

Low Power Register Exchange Viterbi Decoder for Wireless Applications [electronic Resource]

This thesis describes a design and implementation of a Viterbi decoder using FPGA technology. We use the sliding block filtering concept, the pipeline interleaving technique and the forward processing

method to construct the design. We use VHDL to describe the design, Synopsys tools to synthesize it and Xilinx tools to target the design to an XVC300-8 device. Besides the above, the principle of the Viterbi Algorithm, two kinds of structures of the Viterbi decoder, VHDL coding style, a high level synthesis strategy and the methodologies of FPGA design are briefly discussed. We also present complete source code, scripts and reports for this design in appendixes.

This book constitutes the refereed proceedings of the 12th International Conference on Field-Programmable Logic and Applications, FPL 2002, held in Montpellier, France, in September 2002. The 104 revised regular papers and 27 poster papers presented together with three invited contributions were carefully reviewed and selected from 214 submissions. The papers are organized in topical sections on rapid prototyping, FPGA synthesis, custom computing engines, DSP applications, reconfigurable fabrics, dynamic reconfiguration, routing and placement, power estimation, synthesis issues, communication applications, new technologies, reconfigurable architectures, multimedia applications, FPGA-based arithmetic, reconfigurable processors, testing and fault-tolerance, crypto applications, multitasking, compilation techniques, etc.

Proceedings of the ... IEEE International Conference on Electronics, Circuits, and Systems

Index to IEEE Publications

Digital Electronics and Design with VHDL

ACM/SIGDA International Symposium on Field Programmable Gate Arrays

MILCOM '97

Programmable Devices and Systems 2001

This book presents selected research papers on current developments in the fields of soft computing and signal processing from the Third International Conference on Soft Computing and Signal Processing (ICSCSP 2020). The book covers topics such as soft sets, rough sets, fuzzy logic, neural networks, genetic algorithms and machine learning and discusses various aspects of these topics, e.g., technological considerations, product implementation and application issues.

An important working resource for engineers and researchers involved in the design, development, and implementation of signal processing systems The last decade has seen a rapid expansion of the use of field programmable gate arrays (FPGAs) for a wide range of applications beyond traditional digital signal processing (DSP) systems. Written by a team of experts working at the leading edge of FPGA research and development, this second edition of FPGA-based Implementation of Signal Processing Systems has been extensively updated and revised to reflect the latest iterations of FPGA theory, applications, and technology. Written from a system-level perspective, it features expert discussions of contemporary methods and tools used in the design, optimization and implementation of DSP systems using programmable FPGA hardware. And it provides a wealth of practical insights—along with illustrative case studies and timely real-world examples—of critical concern to engineers working in the design and development of DSP systems for radio, telecommunications, audio-visual, and security applications, as well as bioinformatics, Big Data applications, and more. Inside you will find up-to-date coverage of: FPGA solutions for Big Data Applications, especially as they apply to huge data sets The use of ARM processors in FPGAs and the transfer of FPGAs towards heterogeneous computing platforms The evolution of High Level Synthesis tools—including new sections on Xilinx's HLS Vivado tool flow and Altera's OpenCL approach Developments in Graphical Processing Units (GPUs), which are rapidly replacing more traditional DSP systems FPGA-based Implementation of Signal Processing Systems, 2nd Edition is an indispensable guide for engineers and researchers involved in the design and development of both traditional and cutting-edge data and signal processing systems. Senior-level electrical and computer engineering graduates studying signal processing or digital signal processing also will find this volume of great interest.

Proceedings APCC/OECC'99

13th International Workshop on Rapid System Prototyping

Fifth Asia-Pacific Conference on Communications and Fourth Optoelectronics and Communications Conference : [joint Conference Held] October 18-22, 1999, Friendship Hotel, Beijing China

Proceedings of 3rd ICSCSP 2020, Volume 2

Multi-Core Embedded Systems

Implementation of Viterbi Decoder on XILINX XC4005XL FPGA

Proceedings of the June 1996 workshop, focusing on hardware/software codevelopment. Highlights advances in hardware emulation; co- simulation of hardware, software, and mechanical parts; RSP for telecom; and higher level models for system prototyping, and explores subjects including system simulation/emulation in a hierarchical sense, software prototyping and validation, and experiences from specific system prototyping projects. Of interest to system designers, modeling and tool developers, integrated circuit designers, and software engineers. No index. Annotation copyright by Book News, Inc., Portland, OR.

This comprehensive book on application-specific integrated circuits (ASICs) describes the latest methods in VLSI-systems design. ASIC design, using commercial tools and pre-designed cell libraries, is the fastest, most cost-effective, and least error-prone method of IC design. As a consequence, ASICs and ASIC-design methods have become increasingly popular in industry for a wide range of applications. The book covers both semicustom and programmable ASIC types. After describing the fundamentals of digital logic design and the physical features of each ASIC type, the book turns to ASIC logic design - design entry, logic synthesis, simulation, and test - and then to physical design -

partitioning, floorplanning, placement, and routing. You will find here, in practical well-explained detail, everything you need to know to understand the design of an ASIC, and everything you must do to begin and to complete your own design. Features Broad coverage includes, in one information-packed volume, cell-based ICs, gate arrays, field-programmable gate arrays (FPGAs), and complex programmable logic devices (PLDs). Examples throughout the book have been checked with a wide range of commercial tools to ensure their accuracy and utility. Separate chapters and appendixes on both Verilog and VHDL, including material from IEEE standards, serve as a complete reference for high-level, ASIC-design entry. As in other landmark VLSI books published by Addison-Wesley - from Mead and Conway to Weste and Eshraghian - the author's teaching expertise and industry experience illuminate the presentation of useful design methods. Any engineer, manager, or student who is working with ASICs in a design project, or who is simply interested in knowing more about the different ASIC types and design styles, will find this book to be an invaluable resource, reference, and guide.
0201500221B04062001
FPGA-based Implementation of Signal Processing Systems
IFIP TC10 WG10.5 International Conference on Very Large Scale Integration 26–30 August 1997, Gramado, RS, Brazil
The Essentials of Computer Organization and Architecture
Computational Intelligence in Security for Information Systems
Proceedings of the ... IEEE International Workshop on Behavioral Modeling and Simulation
Soft Computing and Signal Processing

Digital Electronics and Design with VHDL offers a friendly presentation of the fundamental principles and practices of modern digital design. Unlike any other book in this field, transistor-level implementations are also included, which allow the readers to gain a solid understanding of a circuit's real potential and limitations, and to develop a realistic perspective on the practical design of actual integrated circuits. Coverage includes the largest selection available of digital circuits in all categories (combinational, sequential, logical, or arithmetic); and detailed digital design techniques, with a thorough discussion on state-machine modeling for the analysis and design of complex sequential systems. Key technologies used in modern circuits are also described, including Bipolar, MOS, ROM/RAM, and CPLD/FPGA chips, as well as codes and techniques used in data storage and transmission. Designs are illustrated by means of complete, realistic applications using VHDL, where the complete code, comments, and simulation results are included. This text is ideal for courses in Digital Design, Digital Logic, Digital Electronics, VLSI, and VHDL; and industry practitioners in digital electronics. Comprehensive coverage of fundamental digital concepts and principles, as well as complete, realistic, industry-standard designs Many circuits shown with internal details at the transistor-level, as in real integrated circuits Actual technologies used in state-of-the-art digital circuits presented in conjunction with fundamental concepts and principles Six chapters dedicated to VHDL-based techniques, with all VHDL-based designs synthesized onto CPLD/FPGA chips

Starts with an overview of today's FPGA technology, devices, and tools for designing state-of-the-art DSP systems. A case study in the first chapter is the basis for more than 30 design examples throughout. The following chapters deal with computer arithmetic concepts, theory and the implementation of FIR and IIR filters, multirate digital signal processing systems, DFT and FFT algorithms, and advanced algorithms with high future potential. Each chapter contains exercises. The VERILOG source code and a glossary are given in the appendices, while the accompanying CD-ROM contains the examples in VHDL and Verilog code as well as the newest Altera "Baseline" software. This edition has a new chapter on adaptive filters, new sections on division and floating point arithmetics, an up-date to the current Altera software, and some new exercises.

Conference Proceedings
FPGA ...
Shortening the Path from Specification to Prototype, June 19-21, 1996, Thessaloniki, Greece
Proceedings : [RSP 2002] : Darmstadt, Germany, July 1-3, 2002
19-22 August, 2001, Singapore
Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology

Papers from a July 2002 workshop describe recent advances in reconfigurable computing, system specification and modeling, distributed prototyping, efficient early evaluation, and prototyping methodologies and tools. Coverage includes prototyping applications ranging from FPGA-based embedded hardware to interactive software systems and networked communication systems; case studies; and topics such as rapid prototyping of FPGA-based floating point DSP systems, prototyping Ethernet in the first mile over point-to-point copper, interfacing software libraries from non-deterministic prototypes, reconfigurable hardware control software, and platform concepts for prototyping and demonstration of high-speed communication systems. This work lacks a subject index. Annotation copyrighted by Book News, Inc., Portland, OR.

The Second International Workshop on Computational Intelligence for Security in Information Systems (CISIS'09) presented the most recent developments in the - namically expanding realm of several fields such as Data Mining and Intelligence, Infrastructure Protection, Network Security, Biometry and Industrial Perspectives. The International Workshop on Computational Intelligence for Security in Infor- tion Systems (CISIS) proposes a forum to the different communities related to the field of intelligent systems for security. The global purpose of CISIS conferences has been to form a broad and interdisciplinary meeting ground offering the opportunity to interact with the leading industries actively involved in the critical area of security, and have a picture of the current solutions adopted in practical domains. This volume of Advances in Intelligent and Soft Computing contains accepted - rd th pers presented at CISIS'09, which was held in Burgos,

Spain, on September 23 -26 , 2009. After a through peer-review process, the International Program Committee selected 25 papers which are published in this workshop proceedings. This allowed the Scientific Committee to verify the vital and crucial nature of the topics involved in the event, and resulted in an acceptance rate close to 50% of the originally submitted manuscripts.

Reduced Complexity Interconnection and Computation for Digital Signal Processing in Communications

CODES+ISSS

Journal of Scientific and Industrial Research

Reconfigurable Computing Is Going Mainstream

Core-Based Behavioral Synthesis

High-speed Viterbi Decoder Design and Implementation with FPGA.

Computer Architecture/Software Engineering

Scientific meetings on programmable devices and systems began in 1995 with the PDS'95 event organised by the Institute of Electronics, Silesian University of Technology (SUT). Many papers on the issues of programmable devices and systems were presented at numerous conferences and workshops devoted to electronics and circuit theory yet there were no workshops devoted solely to those particular topics. Combined with the belief that some specific common problems appeared in the area of PDS justified the decision to organise the PDS meeting. The PDS2001 IFAC Workshop, organised by the Institute of Electronics, SUT, Gliwice, Poland was the 5th event in the series. The aim of the meeting was to define the future trends of this field via the interaction of industry, technical research centres and academia representatives. This Proceedings volume contains 54 duly presented papers and many of them when compared to the Preprints volume version have been corrected and enriched with the discussion results. The papers are grouped according to the Workshop plenary sessions topics as follows: •Communication •Digital Signal Processing •Industrial Programmable Logic Controllers •Field Programmable Logic

Digital Signal Processing with Field Programmable Gate Arrays

International Conference, CSEE 2011, Wuhan, China, August 21-22, 2011. Proceedings